

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Leslie E. Cline et al.

Serial No. 09/751,528

Filed: December 29, 2000

For: PROCESSOR PERFORMANCE
STATE CONTROL

Director of U.S. Patent and Trademark Office
Alexandria, VA 22313-1450



Examiner: C. W. Chung

Art Unit: 2115

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JUN 09 2004

Technology Center 2100

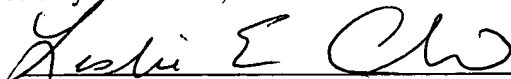
DECLARATION UNDER 37 C.F.R. §1.131

- Leslie E. Cline, Xia Dai, Varghese George, and Robert L. Farrell hereby declare that:
1. We are the co-inventors of the above-captioned patent application and the subject matter described and claimed therein.
 2. Prior to December 13, 2000, we the undersigned conceived and reduced to practice the invention described and claimed in the above-captioned patent application (hereinafter, "the present invention"), as shown by the Exhibit attached to this declaration. The Exhibit is an Invention Disclosure form submitted by us to our employer located in the United States prior to December 13, 2000. The dates on the Exhibit have been redacted. Each of the redacted dates on the Exhibit are prior to December 13, 2000.
 3. Intel Corporation is the assignee of the present invention.

We hereby declare that all statements herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made knowing that willful false statements and the like are punishable by fine or imprisonment, or both under § 1001 of Title 18 of United States Code, and such willful or false statements may jeopardize the validity of the above-identified application or any patent issuing therefrom.

Respectfully submitted,

Date: May 3, 2004


Leslie E. Cline

Date: _____, 2004

Xia Dai

Date: _____, 2004

Varghese George

Date: _____, 2004

Robert L. Farrell

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Date: _____, 2004

Leslie E. Cline

Date: 04/29, 2004


Xia Dai

Date: _____, 2004

Varghese George

Date: _____, 2004

Robert L. Farrell

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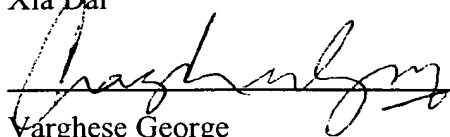
Date: _____, 2004

Leslie E. Cline

Date: _____, 2004

Xia Dai

Date: 4/30/, 2004



Varghese George

Date: 4/29/, 2004



Robert L. Farrell

15 + 15 P10231

INTEL INVENTION DISCLOSURE
ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

AUG - 1 2000

DATE: July 27, 2000

JUN 07 2000

Mobile
Platforms / IAGI MPG

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed and signed, please return this form to the Legal Department at 8-0444. If you have any questions, please call 264-0444.

1. Inventor: Cline Leslie E
Last Name First Name Middle Initial
Phone 408-765-7066 M/S: RN6-49 Fax # 408-765-4614
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Supervisor* Sung-Soo Cho WWID 10038632 Phone 408-765-5264 M/S: RN6-49

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JUL 31 2000

PATENT DATABASE GROUP

INTEL LEGAL TEAM

Inventor: Dai Xia
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Supervisor* Pochang Hsu WWID 10074343 Phone 408-765-6772 M/S: RN6-52

office address 350 East Plumeria Dr., San Jose, CA 95134

CHP 3-108

Inventor: George Varghese
Last Name First Name Middle Initial
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*Corporate Level Group (e.g. IABG, NCG, CEG) IABG Division MPG Subdivision 100-7511-6
Supervisor* Joe Skupnjak WWID 10017794 Phone 356-5025 M/S: FM5-162

Inventor: Farrell Robert L
Last Name First Name Middle Initial
Phone 916-356-3855 M/S: FM5-162 Fax # 916-345-2205
Citizenship: USA WWID: 10034296 Contractor: YES NO X
Inventor E-Mail Address: Robert.L.Farrell@intel.com
Home Address: 2167 Promontory Point Lane
City Gold River State CA Zip 95670 Country USA
*Corporate Level Group (e.g. IABG, NCG, CEG) IABG Division MPG Subdivision 100-7511-6
Supervisor* Joe Skupnjak WWID 10017794 Phone 356-5025 M/S: FM5-162

*If you are unsure of this information, please discuss with your manager.

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: M & A for Intel® SpeedStep™ technology Direct Processor Performance State control.
-
3. What technology/product/process (code name) does it relate to (be specific if you can):
CPU Geyserville technology, defines a new method for software to select Geyserville states.
-
4. Include several key words to describe the technology area of the invention in addition to # 3 above: Intel® SpeedStep™ Technology, Processor Performance State, ACPI 2.0 Specification.
-
5. Stage of development (i.e. % complete, simulations done, test chips if any, etc.): Concept is 100% complete, currently appears unlikely that this idea will be used in any Intel products in the near future (might be used by other CPU vendor(s)).
-
6. (a) Has a description of your invention been, or will it shortly be, published outside Intel:
NO: X YES: _____ If YES, was the manuscript submitted for pre-publication approval? _____
IDENTIFY THE PUBLICATION AND THE DATE PUBLISHED: _____
- (b) Has your invention been used/sold or planned to be used/sold by Intel or others?
NO: X YES: _____ DATE WAS OR WILL BE SOLD: _____

- (c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification? NO: X YES: _____

NO: X YES: _____ Name of SIG/Standard/Specification: _____

- (d) If the invention is embodied in a semiconductor device, actual or anticipated date of tapeout? not currently expected to be used by Intel, but might be used by other CPU vendor(s).

- (e) If the invention is software, actual or anticipated date of any beta tests outside Intel _____

7. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia? NO: X YES: _____ Name of individual or entity: _____

8. Is this invention related to any other invention disclosure that you have recently submitted? If so, please give the title and inventors: no

**PLEASE READ AND FOLLOW THE DIRECTIONS ON
HOW TO WRITE A DESCRIPTION OF YOUR INVENTION**

Please attach a description of the invention to this form, DATED AND SIGNED BY AT LEAST ONE PERSON WHO IS NOT A NAMED INVENTOR, and include the following information:

1. **Describe in detail what the components of the invention are and how the invention works.**

The ACPI 2.0 Specification defines a Processor Performance State capability, and a software interface that the operating system can use to dynamically change the processor performance/power characteristics, based on a software policy implement in the operating system. The software interface uses an integer number to specify the use of an arbitrary number of processor performance states, P0 through Pn."

This invention is a CPU internal control register interface to software, that directly corresponds to the ACPI 2.0 Specification Processor Performance State format, coupled with a method to associate the integer number with CPU core frequency and core power supply voltage. The integer number acts as a pointer into an internal CPU read-only memory table, that holds unique information for CPU core frequency and core power supply voltage for each of the Processor Performance States implemented by the CPU.

2. **Describe advantage(s) of your invention over what is done now.**

This invention considerably simplifies the current control method, by moving the control method from the chipset to the CPU, and reducing the software interface to communicating an integer number. Also, it permits CPU implementation of an arbitrary number of CPU performance/power states, and insures optimal CPU core frequency and core power supply voltage for each of these states

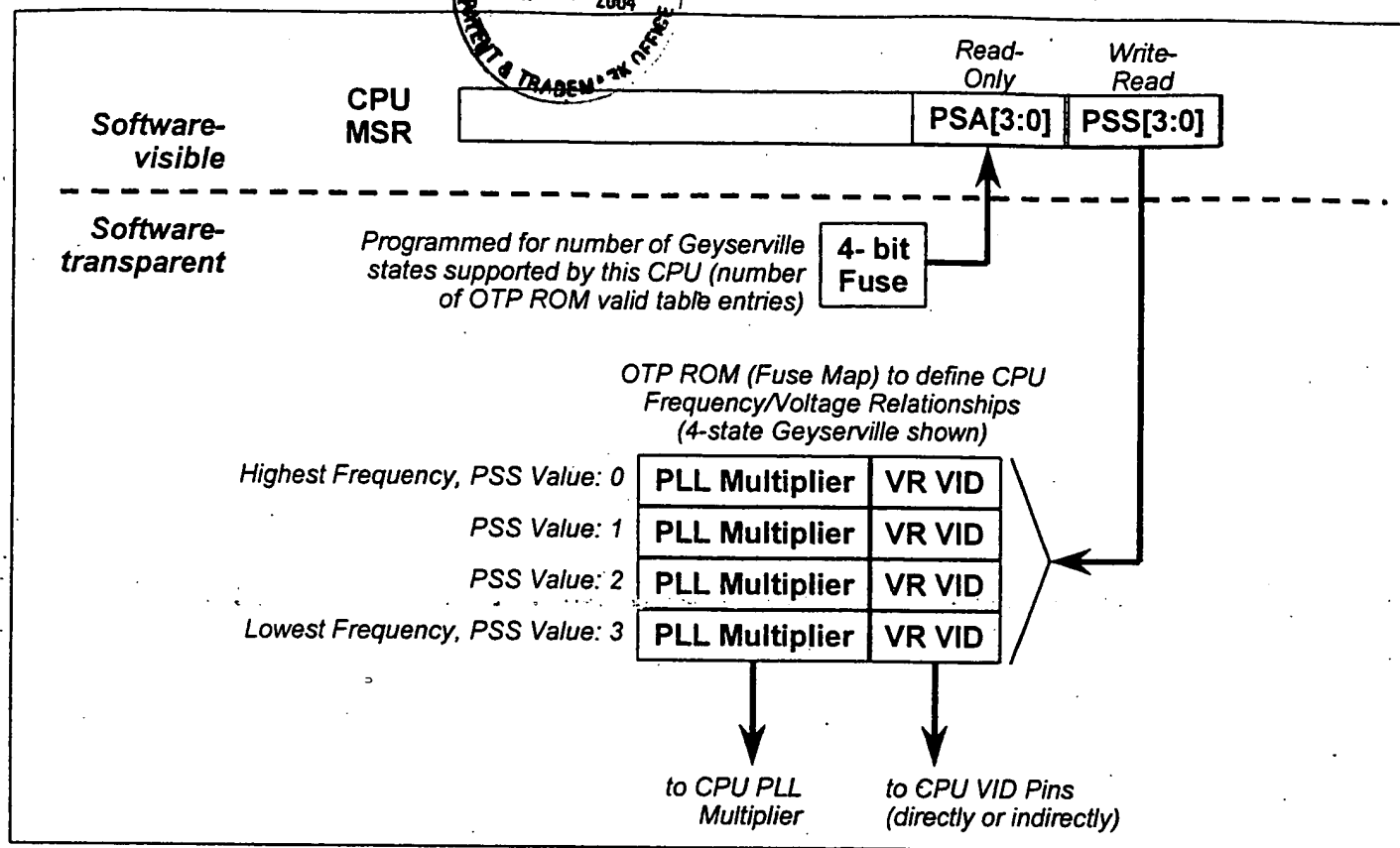
3. **YOU MUST include at least one figure illustrating the invention.
If the invention relates to software, include a flowchart
or pseudo-code representation of the algorithm.**

This figure and description shows one possible implementation of this invention.

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The CPU MSR is a control register in the CPU. The PSA[3:0] read-only bit field informs the control software of the number of Processor Performance States supported by this CPU. In this example, the 4-bit Fuse is programmed to a binary value of 0011b, to indicate that this CPU supports Processor Performance States P0, P1, P2 and P3. The PSS[3:0] write/read bit field can be read by the control software to learn the current Processor Performance State, and written by the control software to select a new Processor Performance State. In this example, valid values binary values are 0000b, 0001b, 0010b and 0011b, directly corresponding to the Processor Performance States P0-P3.

In this example, the PSS[3:0] binary value is used as an address to the OTP ROM array, to select one of the PLL Multiplier and VR VID values. When a new PSS[3:0] value is written, a method beyond the scope of this invention is used to change the CPU core frequency (defined by the PLL Multiplier value sent to the CPU internal clock generator PLL) and CPU core power supply voltage (as defined by the VR VID value).

The PLL Multiplier and VR VID values are defined to deliver optimal CPU performance/power relationships for the various possible Processor Performance States. While an OTP ROM implemented with CPU Fuses is shown in this example, other technologies are possible, including CPU microcode or software loading of this information during CPU initialization or shortly after CPU Reset.

4. Value of your invention to Intel (how will it be used?).

This technology could be used by Intel in future CPUs, if a need is found for directly implementing all CPU core frequency/voltage relationships in CPU hardware. Also, it is possible that this invention could be independently developed by other CPU vendors.

5. Explain how your invention is novel. If the technology itself is not new, explain what makes it different.

Current and planned future CPU Geyserville control methods do not provide CPU hardware-enforced restrictions on CPU frequency/voltage relationships. Instead, these relationships are either hard-wired in platform hardware,

or are determined by software. In either case, it is possible for non-optimal CPU frequency/voltage relationships to be applied to the CPU. With this invention, it is not possible to apply non-optimal CPU frequency/voltage relationships to the CPU, because only optimal relationships are defined within the CPU hardware.

6. Identify the closest or most pertinent prior art that you are aware of.

This invention is an alternative control method for CPU Geyserville frequency/voltage control, which has been disclosed in a number of previous invention disclosures.

7. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

Manufacturers of CPU devices. Infringement would be identified by advertisement or use of a "Direct ACPI 2.0 Processor Performance State control interface."

***HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM**

DATE: 7/28/2000 SUPERVISOR: *Singler Chr*

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID

P10231

INTEL CONFIDENTIAL

INTEL INVENTION DISCLOSURE

AUG - 2 2000

LEGAL ID# 15931

Mobile
Platform IAG/MPG
JUN 07 2004

DATE: July 28, 2000

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to the Legal Department at JF3-147. If you have any questions, please call 264-0444 or 264-0998.

1. Inventor: Dai Xia (Kevin)
 Last Name First Name Middle Initial
 SS# 471-25-8371 WWID 10177836 Phone 765-7560 M/S: RN6-52 h
 Home Address: 1423 Chavez Way City San Jose State CA Zip 95131
 Citizenship: P.R.C. BUM Presenter: Frank Spindler
 Group: (e.g. TMG, ICG, CEG) IABG Division Name MPG Subdivision 100-7021-6
 Supervisor* Pochang Hsu WWID 10074343 Phone 765-6772 M/S: RN6-52

Inventor: _____
 Last Name First Name Middle Initial
 SS# _____ WWID _____ Phone _____ M/S: _____
 Home Address: _____ City _____ State _____ Zip _____
 Citizenship: _____ BUM Presenter: _____
 Group: (e.g. TMG, ICG, CEG) IABG Division Name MPG Subdivision 100-7021-6
 Supervisor * _____ WWID _____ Phone _____ M/S: _____

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Method and Apparatus of CPU based Geyserville control
 3. What technology/product/process (code name) does it relate to: Intel future Mobile/Server CPU products
 4. Stage of development (i.e. % complete) 50 %

5. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

NO: x YES: _____ DATE WAS OR WILL BE PUBLISHED: _____

If YES, was the manuscript submitted for pre-publication approval? YES: _____

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 AUG 04 2000
 PATENT DATABASE GROUP
 INTEL LEGAL TEAM

- (b) Has your invention been used/sold or planned to be used/sold by Intel or others?

NO: _____ YES: x DATE WAS OR WILL BE SOLD: _____

- (c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?

NO: x YES: _____ Name of SIG/Standard/Specification: _____

- (d) If the invention is a semiconductor device, actual or anticipated date of tapeout? _____

- (e) If the invention is software, actual or anticipated date of any beta tests. _____

6. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia?

NO: x YES: _____ Name of individual or entity: _____

**PLEASE READ AND FOLLOW THE DIRECTIONS ON THE ATTACHED
 PAGE ON HOW TO WRITE A DESCRIPTION OF YOUR INVENTION**

1. Describe in detail how the invention works.
 - a) The purpose of this invention is to offer a M&A for CPU based Geyserville control
 - b) Hardware consists of 3 parts-BR/VidTargets, VidROM and control.
 - c) BR/VidTargets consists of all the Bus Ratio's and corresponding Vid Targets that comprising the Geyserville states. It is a fuse block that is programmed after testing is done. The bus ratio-Vid targets setting and relationship is processor segment dependent, processor stepping dependent and bin group dependent.
 - d) VidROM is a ROM that has all the Vid entries that controls the VR.
 - e) Control hardware consists of a up-down counter, a comparator and a finite state machine(FSM).
 - f) When CPU starts a Geyserville transition, it first instructs FSM the target state index. FSM will then read out the corresponding bus ratio and Vid target pair. Bus ratio will be passed to PLL block. Vid target will be passed to comparator.
 - g) For a low to high transition, voltage will be raised before switching CPU core frequency. For a high to low transition, CPU will switch core frequency and then lowers the voltage.
 - h) Voltage ramping is a process controlled through comparator, Up-down counter and VidROM, . The comparator compares the target Vid with the current Vid. The Up-down counter will walk the VidROM one step at a time until the current Vid reaches the target Vid. VidROM output will be passed to VRM.
 - i) Since voltage ramping rate can be controlled through FSM by adjusting Up-down counter update rate, handshaking between VRM and CPU can be eliminated. CPU will wait long enough for each 25mV~50mV Vid step to be fulfilled by VRM
2. Describe advantage(s) of your invention over what is done now.

Current VRM control is done through VCH and on board Vid wiring. It is a workable solution for a 2 state Geyserville architecture, but for multiple states Geyserville, this scheme complicates platform design. The proposed scheme enables a CPU based Geyserville control interface that offers platform simplicity, safety as well as ease of management. ICH will no longer be part of the Geyserville control loop, No more on board wiring is needed; binding of bus ration-Vid pairs through fuse also eliminates illegal frequency-voltage combinations that may either damage CPU oxide through over voltage or cause a CPU function failure when voltage level is insufficient for the operating frequency. The scheme also frees ACPI/OS/ICH/board wiring from managing bus ratio and Vid pairs that is processor segment dependent, processor stepping dependent and bin group dependent. Handshaking between VRM and CPU can also be eliminated due to stepwise Vid ramping under predefined rate control.
3. Include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.
4. Value of your invention to Intel (how will it be used?).

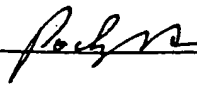
The invention proposes value added power management feature for Intel mobile CPU. When used on mobile platform, it can offer platform simplicity, safety as well as ease of management.
5. Identify the closest or most pertinent prior art that you are aware of.

N/A
6. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?

This feature is a key feature CPU power management state and can be identified by product spec.

*HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM

DATE: 9/31/00

SUPERVISOR: 

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS
DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID



6 June, 2000



Geyll Vid Scheme

Development Group

- CPU controlled dynamic Vid
 - CPU based scheme can bind bus ratio with Vid in production
 - stepping dependant, bin group dependant
- Use ROM to generate Vid output
 - Using ROM saves fuse resource
 - Vid table has $32 \times 5 = 160$ bits
 - Using ROM eliminates illegal Vid
 - a register based scheme will be prone to software bug
 - register scheme involves read and write
 - ROM only involves read
 - ROM can limit the upper and lower Vid values
 - avoid over voltage or under voltage

intel

6 June, 2000

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1



Index/BusRatio/Vid Fuse Field

Development Group

- Geyserville States has three field
 - Index Field: used for MSR read BusRatio/Vid tagging
 - BusRatio Field: used for PLL lock
 - VidTarget Field: used for matching voltage with frequency
- MSR act as liaison between software and hardware
 - MSR accesses Index field to read out number of states
 - MSR read index field
 - MSR pass the index to ACPI
 - BIOS can mask out certain Geyserville states
 - ACPI uses MSR to designate target state
 - ACPI writes MSR
 - MSR pass the index to FSM
 - FSM use the index to read out BR/Vid pair

intel

6 June, 2000

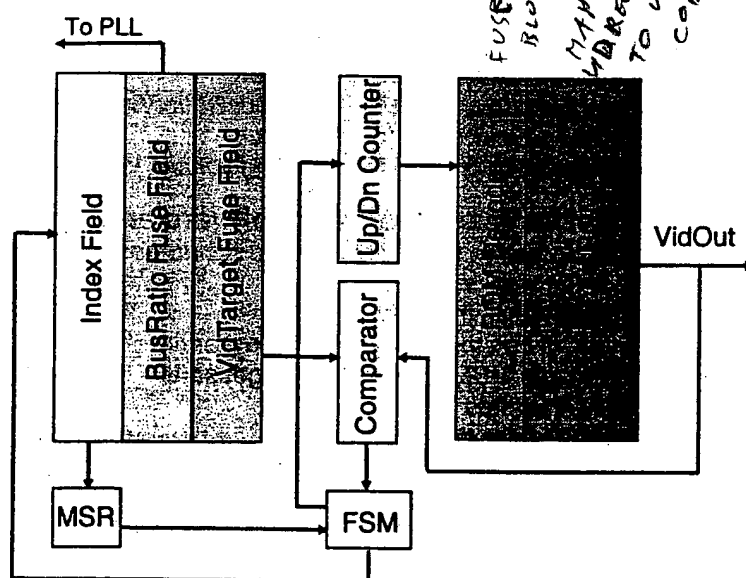
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2

Geyserville Configuration Block

GeyMode	Index	BusRatio	VidTarget
ReserveMode	00-	xxxx/yyyy(00)	zzzzz(00)
BatMode	01-	xxxx/yyyy(01)	zzzzz(01)
ACMode	10-	xxxx/yyyy(10)	zzzzz(10)
TurboMode	11-	xxxx/yyyy(11)	zzzzz(11)

Vid Block Diagram



P10231

INTEL INVENTION DISCLOSURE

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AUG - 2 2000

LEGAL ID# 15934

Mobile
Platform / IAG

JUN 07 2000

DATE: July 28, 2000

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 Citizenship: P.R.C. BUM Presenter: Frank Spindler
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 Supervisor* Pochang Hsu WWID 10074343 Phone 765-6772 M/S: RN6-52

Inventor: Cline Leslie E
 Last Name First Name Middle Initial
 Phone 408-765-7066 M/S: RN6-49 Fax # 408-765-4614
 Citizenship: USA WWID: 10580426 Contractor: YES NO X
 Inventor E-Mail Address: Les.Cline@intel.com
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 Corporate Level Group (e.g. IABG, NCG, CEG) IABG Division MPG Subdivision 100-7021-6
 Supervisor* Sung-Soo Cho WWID 10038632 Phone 408-765-5264 M/S: RN6-49

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Method and Apparatus of CPU based VRM control and software based Geyserville interface

3. What technology/product/process (code name) does it relate to: Intel future Mobile/Server CPU products

4. Stage of development (i.e. % complete) 50 %

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NO: x YES: DATE WAS OR WILL BE PUBLISHED: AUG 04 2000

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(d) If the invention is a semiconductor device, actual or anticipated date of tapeout?

(e) If the invention is software, actual or anticipated date of any beta tests.

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NO: x YES: Name of individual or entity:

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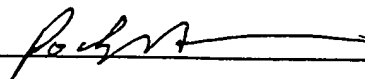
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 - c) VidROM is a ROM that has all the Vid entries that controls the VR.
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 - g) Voltage ramping is a process controlled through comparator, Up-down counter and VidROM, . The comparator compares the target Vid with the current Vid. The Up-down counter will walk the VidROM one step at a time until the current Vid reaches the target Vid. VidROM output will be passed to VRM.
 - h) Since voltage ramping rate can be controlled through FSM by adjusting Up-down counter update rate, handshaking between VRM and CPU can be eliminated. CPU will wait long enough for each 25mV~50mV Vid step to be fulfilled by VRM.
2. Describe advantage(s) of your invention over what is done now.
 Current VRM control is done through VCH and on board Vid wiring. It is a workable solution for a 2 state Geyserville architecture, but for multiple states Geyserville, complexity and overhead piles up. The proposed scheme enables a CPU based VRM control interface that offers platform simplicity as well as ease of management. ICH will no longer be part of the Geyserville control loop; No more on board wiring is needed; CPU can have as much as possible Geyserville state without hardware overhead. Handshaking between VRM and CPU can also be eliminated due to stepwise Vid ramping under predefined rate control.
3. Include at least one figure illustrating the invention. If the invention relates to software, include a flowchart or pseudo-code representation of the algorithm.
4. Value of your invention to Intel (how will it be used?).
 The invention proposes value added power management feature for Intel mobile CPU. When used on mobile platform, it can offer platform simplicity, Geyserville feature flexibility.
5. Identify the closest or most pertinent prior art that you are aware of.
 N/A
6. Who is likely to want to use this invention or infringe the patent if one is obtained and how would infringement be detected?
 This feature is a key feature CPU power management state and can be identified by product spec.

*HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM

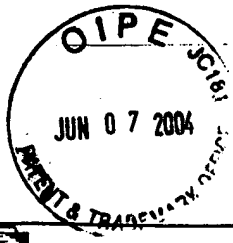
DATE:

7/31/00


SUPERVISOR:



BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID




6 June, 2000



Development Group

GeylII Vid Scheme

- CPU controlled dynamic Vid
 - ◆ Use ROM to generate Vid output
 - ◆ Using ROM saves fuse resource
 - Vid table has $32 \times 5 = 160$ bits
 - ◆ ROM can limit the upper and lower Vid values
 - avoid over voltage or under voltage
- MSR contains two fields for Geyserville
 - ◆ BusRatio Field: used for PLL lock
 - ◆ VidTarget Field: used for providing target Vid for VidROM
- MSR acts as liaison between software and hardware
 - ◆ ACPI uses MSR to designate target state
 - ACPI writes MSR bus ratio and target Vid
 - MSR passes the bus ratio to PLL and target Vid to VidROM



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Intel Confidential

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